C: Remarks:

The present amendment is filed formally in accordance with the examiner's suggestions which are appreciated and to place this application in condition for allowance. The examiner is thanked for the suggestions. The second Claim 27 was RENUMBERED 31 AND CANCELED because the subject matter was moved into claim 1. As required by the Examiner, Figure 8 has been added to particularly illustrate the case of claim 9, and corresponding changes have been made in the specification. Figure 9 illustrates particularly the subject matter of claims 26 and 27 and when combined with Figure 10, Figures 9 and 10 illustrate particularly Claims 15, 16, 17 and 18. Corresponding changes have been made in the description.

In answer to the examiners question about the use of purge in the claim, which use was correct, and to answer the examiner's question it has been decided to combine the duplicate second claim 27 into claim 1, as that language is true for all claims and makes the use of purge in claim 1 clear to the person of ordinary skill in the art. Indeed purging occurs even though the moving of a coherency region from one set of processing nodes to another effectively leaves behind cache entries on the old nodes and that cache entries for the same main storage address will not be established in the new nodes until the old entries are invalidated.

THE EXAMINER IS THANKED FOR NOTING THAT EXTRANEOUS MATERIAL HAD BEEN INCORPORATED IN THE PRIOR RESPONSE. The above comments are confirmed. Extraneous material has been deleted.

The remarks included answer to the examiners question about the use of purge in the claim, which use was correct, and to answer the examiner's question it has been decided to combine the duplicate second claim 27 into claim 1, as that language is true

for all claims and makes the use of purge in claim 1 clear to the person of ordinary skill in the art. Indeed purging occurs even though the moving of a coherency region from one set of processing nodes to another effectively leaves behind cache entries on the old nodes and that cache entries for the same main storage address will not be established in the new nodes until the old entries are invalidated. Because of this and because of the amendment to claim 1 adding the limitation in claim 1 about "and when moving a software process between two distinct sets of processing nodes a cache line cannot be marked as shared in two separate coherency regions, and when said supervisor program is moving a coherency region from one distinct set of processing nodes to another distinct set of processing nodes it is effectively leaving behind cache entries for the coherency region on the old nodes and ensures that these old cache entries will be seen by incoming storage requests originating from the new processing nodes and that cache entries for the same main storage addresses will not be established in the new processing nodes until the old entries are invalidated" makes the rejection under 102(b) moot.

As to Cypher 7032078 the present invention requires less overhead in the supervisor software. This applicatino uses just the history of which physical procesors have been used for the dispatch of logical processors to make the correct settings of the choherency mode bits during dispatch. The invention does notu use addrss mappings to determine which processors are requried to snoop broadcast requests, but works directly from the hypervisors internal map of logical processors to physical processors. This avoid the manipulation of the address entries in Cypher's mode table (Fig. 2, 260).

In this application the hypervisor keeps track of whether a process has been moved from one coherency regision to another. Storage requests are sent to the chaches in a new cohernecy

regision. If a new coherency regsion rsults in a complete miss then the request is forwarded to all of the processors that are outside the new region. If the request hits in a cache that is outside of the new regsion then those caches can see that the request was part of a two phase request and they know to discard their cached copies. Thus "when moving a software process between two distinct sets of processing nodes a cache line cannot be marked as shared in two separate coherency regions, and when said supervisor program is moving a coherency region from one distinct set of processing nodes to another distinct set of processing nodes it is effectively leaving behind cache entries for the coherency region on the old nodes and ensures that these old cache entries will be seen by incoming storage requests originating from the new processing nodes and that cache entries for the same main storage addresses will not be established in the new processing nodes until the old entries are invalidated".

Accompanying the prior July 18, 2007 Amendment was a Terminal Disclaimer for this application disclaiming any term after the expiration of the related patent application USSN 10/603,251 when it issues as a patent.

REPLACEMENT SHEETs were in the prior response submitted for the first three Figures of drawings and NEW SHEETs are submitted for the required new drawings 8, 9 and 10. The supporting text is inserted on page 15 of the specification.

Accompanying the prior Amendment was a Terminal Disclaimer for this application disclaiming any term after the expiration of the related patent application USSN 10/603,251 when it issues as a patent.

A notice of allowance is respectfully requested.

RESPECTFULLY SUBMITTED
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